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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/056,193	01/24/2002	Dirgha Khatri	2008.003800	3821

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EXAMINER	
NGUYEN, VIET Q	
ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 07/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/056,193	Applicant(s) KHATRI ET AL.	
	Examiner Viet Q Nguyen	Art Unit 2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Election filed on 1/24/02* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-61* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1- 4, 9-14, 16-22, 27-30, 32, 34-37, 42- 46, 51-54, 56, 58-61* is/are rejected.

7)☒ Claim(s) *5-8,15,23-26,31,33,38-41,47-50,55 and 57* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The applicant's election of claims 1-58 of Group 1 have been acknowledged and made of record.

Claims **1-58** are present for examination.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim **1- 4, 9-14, 16-22, 27-30, 32, 34-37, 42- 46, 51-54, 56, 58-61** are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (6,256,235) and Karabatsos et al (6266252) and Taguchi et al (5,955,889) and Perino et al (6,067,594) and Grundon et al (6,510,100).

Lee see fig. 1) teaches a memory module including a plurality of memory devices (13A-13D) which connected to a connector bus(8), and a plurality of lines (64) coupling such devices to the connector (8), and a termination circuitry including a pull-up resistor (17) and a voltage generator (UTT) coupled to at least a subset of the lines (64) as claimed.

Karabatsos(see fig.1) teaches a memory module including a plurality of memory devices (10, 12, 14) which connected to a connector (5), and a plurality of lines (18, 22) coupling such devices to the connector (5), and a termination circuitry (chip 80, 82, see fig. 4) coupled to at least a subset of the lines through the switches (86, 886) as claimed. Karabatso also shows the use of connector edge (8) for these memory circuits cards 10, 12, 14) connected to the bus substrate as one of the expansion socket as shown.

In regard to claims 59-61, Fig. 1 also shows that there are plurality of expansion sockets (8) on the substrate mother board (28). Note that the use of switch ICs (86, 88, see Fig.4) is selectable by the enabling signals lines (FETenable1 and enable2) in order to selectively disabling or enabling a termination circuitry , thus also disabling or enabling corresponding DIIM card' termination circuitry (80, 82) as claimed. Thus, the claimed step of "setting a switch on one of the expansion board is obviously suggested in this reference also.

Taguchi et al(see fig. 1) teaches a memory module including a plurality of memory devices (SDRAM) which connected to a connector bus(DQ 1), and a plurality of lines (10, 31-34) coupling such devices to the connector bus (DQ1), and a termination circuitry including a pull-up resistor (2) coupled to at least a subset of lines (31-34) as claimed.

Perino et al (see fig. 4) teaches a memory module including a plurality of memory devices (420) which is obviously connected to a connector bus not shown (on the substrate and the edge 430), and a plurality of lines (450) coupling such devices to the connector edge on the substrate, and a termination circuitry including a pull-up resistor (440) coupled to at least a subset of the lines (450) as claimed. It would have been obvious that each memory card has its edge connecting the bus on the substrate, if any, to the memory chip controller (400) as shown.

Grundon et al (see fig. 1) teaches a memory module including a plurality of memory devices (DIMM 40), which connected to a connector bus on the substrate. Further, Fig.5 shows in detail one of such circuit memory device (40 which includes a connector bus(29) onto the substrate for I/O data connection, and at least one of the coupling clines (246) for connecting the shown memory (4) to the connector bus (290), and a termination circuitry including a pull-up resistor (246) and a voltage generator (Vcc) coupled to at least a subset of the lines (246) as claimed

3. Other claims contain allowable subject matter over prior arts of record.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Viet Q Nguyen whose telephone number is (703) 308-4897. The examiner can normally be reached on 7-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (703) 308-4897. The fax phone numbers

for the organization where this application or proceeding is assigned are (703) 308-7724 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

V. Nguyen

Viet Q Nguyen
Primary Examiner
Art Unit 2818

V. Nguyen
July 14, 2003